# Design of Reversible Decoder Using QCA Technology

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**Abstract – A decoder is imperative piece of memory, for address decoding and encoding. The scaling influences the gadget execution because of limitations like warmth dispersal and power utilization. A Quantum dot Cellular Automata (QCA) is a contrasting option to CMOS.QCA offers higher speed, bring down power utilization and higher thickness. In non reversible gates some measure of force misfortune is included. Enthusiasm for reversible rationale offers decreased warmth scattering and builds the speed. It is another transistor-less calculation in nanotechnology. In this venture propose a reversible gate based decoder design. It gives reversibility and area minimization. A QCA designer tool has been used to approve the execution of reversible decoders.**

**Index Terms – Quantum Dot Cellular Automata (QCA), Complementary Metal Oxide Semiconductor (CMOS), Reversible Gates.**

## 1. INTRODUCTION

The measure of Complementary Metal Oxide Semiconductor (CMOS) transistor continues contracting to expand the thickness on chip as per Moore's Law [1]. In CMOS technology, its feature size has diminished after several decades [2]. On the other hand, a couple of impediments still exit. This has brought about the quick advancement of atomic plans on the nanoscale. QCA is one of the options in nanotechnologies for FFT based device. It is relied upon to accomplish low zone and power utilization and high exchanging speed. It has no voltage source and the position of electrons decides the sensible qualities.

QCA cell comprise of four quantum dots arranged in square pattern [3]. Every cell has two electrons which are freed to passage to nearby spots. Electrons tend to keep furthest separation between each other, they live corner to corner to each other because of equal electrostatic awful constrain between them. Cell has two unique states, spoke to by rationale 0 and rationale 1 [4].

Reversible circuits don't lose any data, and it can be create special yield vector from every info vector. Landauer demonstrated that joules of vitality are created for every piece of data lost because of nonreversible calculation; vitality scattering would not really happen in reversible calculation. In Reversible gate, there is coordinated mapping between the information and yield which is not the situation with traditional basis. Utilizing this reversible rationale we can recover contribution from yield and the quantity of information lines is equivalent to number of yield lines.

In this paper a productive way to deal with examination and outline of decoder with reversible NAND gateway utilizing Quantum dot Cell Automata. This paper we utilize the greater part gates is the basic segment of the QCA circuit execution. The reversible decoder circuit is outlined and reproduction results are broke down utilizing QCA designer tool. This test system device is more valuable for building a troublesome decoder input levels. The proposed structure of reversible decoder required a decreased number of dominant part entryway capacities.

## 2. RELATED WORKS

In past, plan strategies for line decoders are CMOS, transmission entryway logic, pass transistor double esteem logic, mixed logic [5]. Two new topologies are given for the 2-4 decoders: a 14-transistor topology pointing on diminish the transistor check and power dissemination, a 15-transistor topology pointing on high power-postpone execution. Both an ordinary and an upsetting decoder are executed for every situation, gives a sum of four new outlines. Besides, four novel 4-16 decoders are outlined, by utilizing blended rationale 2-4 predecoders joint with standard CMOS post-decoder. All proposed decoders have full variance capacity and decreased transistor number contrasted with their normal CMOS partners. Usage of four 4-16 decoders by utilizing the four new 2-4 as predecoders are consolidated with CMOS NOR/NAND entryways to create the decoded yields [5].

The new topologies got from this mix are:

A.4-16LP appeared in Fig.2.1, the two 2-4LPI predecoders consolidated with a NOR-based post-decoder.

B.4-16HP appeared in Fig.2.2 ,the two 2-4HPI predecoders joined with a NOR-based post-decoder

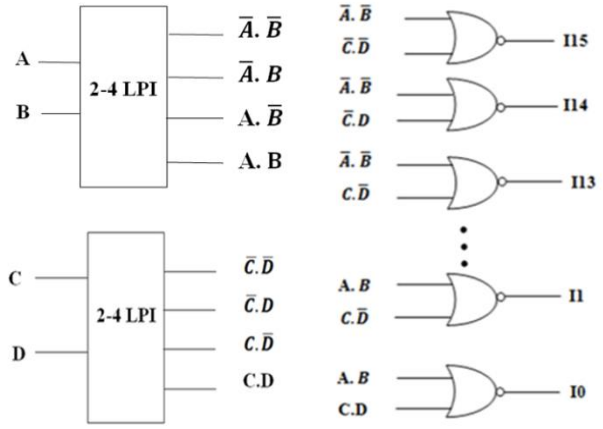



Figure 2.1. A 4-16 LP Decoder

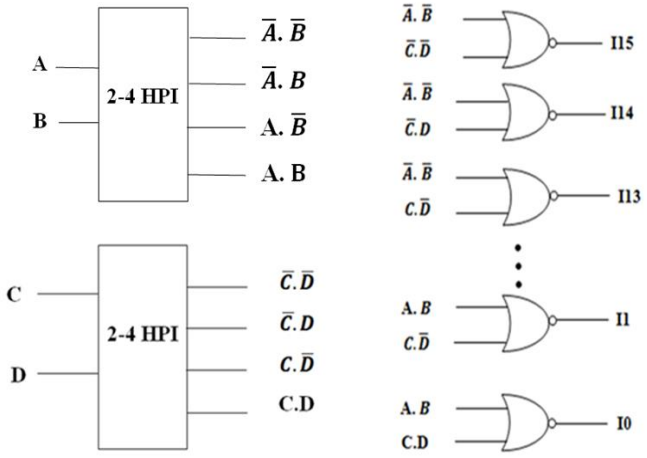



Figure 2.2. A 4-16 HP Decoder

C.4-16HPI appeared in Fig.2.3, the two 2-4HP predecoders joined with a NAND-based post-decoder.

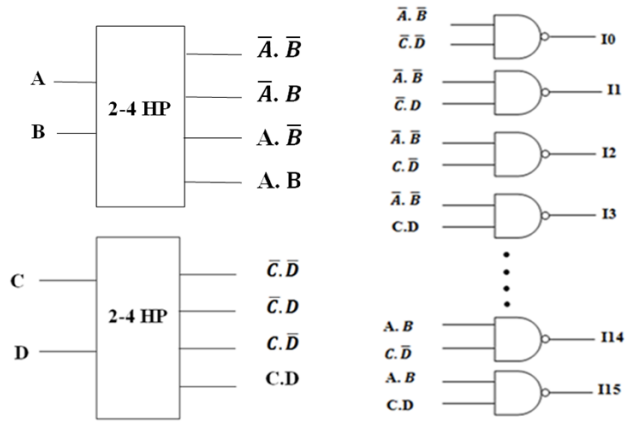



Figure 2.3 A 4-16 HPI Decoder

D. 4-16LPI appeared in Fig.2.4, the two 2-4LP predecoders joined with a NAND-based post-decoder

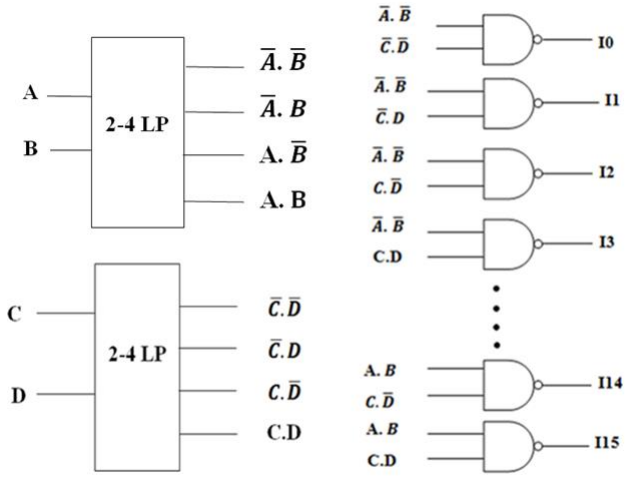



Figure 2.4. A 4-16 LPI Decoder

In the scaling procedure some second request gadget attributes, for example, sub threshold operation, are generally overlooked or gave careful consideration, and their cancelation is more sought than their change. Crisscross in CMOS gadgets is generally high. This is uncommonly preventing the unwavering quality of simple preparing in vision chips. Here one of the primary troubles in CMOS is quantum burrowing through covers, bringing on spillage streams that expansion control utilization.

A standout amongst the most encouraging nanotechnologies which can supplant the present transistor based CMOS innovation is the Quantum-Dot Cellular Automata. The real preferences of this innovation are lesser power dispersal, enhanced speed and thick structures. As of now all rationale doors depend on CMOS innovation. With the present pace of scaling CMOS innovation is set to hit a detour in the following couple of years, where it can't be further downsized because of a few reasons like passage streams, quantum impacts, sub threshold spillage, short channel impacts, creation costs and interconnect delay and so forth. Rationale Design with Quantum Dots is a standout amongst the latest advances being inquired about which permits scaling to keep on atomistic measurements.

Not at all like calculation components that include the exchange of electrons, as in CMOS entryways, does QCA calculation not include electron exchange between nearby QCA cells. Subsequently control dissemination is less in circuits composed with QCA cells. Since just couple of electrons is included in QCA calculations, it is powerless to warm issues. In this way it is critical to consider control as an essential parameter amid the QCA outline prepare.

The power loss in timed QCA circuits are delegated exchanging power and leakage power.. Power loss is free of info states and happens when the clock vitality is raised or brought down to

energize or depolarize a cell. Exchanging power wards on info information and happens when the cell changes the state. Add up to power loss can be controlled by fluctuating the rate of progress of moves in the timing capacity [4].

## 3. PROPOSED METHOD

Here a powerful way to analyze and design of decoder with reversible NAND gate, which utilizing quantum dot cell automata in nanoscale. This paper we utilize the larger part gate is the principal segment of the QCA circuit execution. The proposed circuit is designed and simulated using quantum dot cell automata designer tool, furthermore this test system tool is more helpful for building an intricate info levels. The proposed structure required just less number of greater part gate capacities contrasted with past structures.

### A. Feynman Gate

Feynman gate is a fundamental reversible gate; It has two sources of info and two yields [6]. To start with yield is same as the information and the other is XOR of contributions as appeared in Fig.3.1

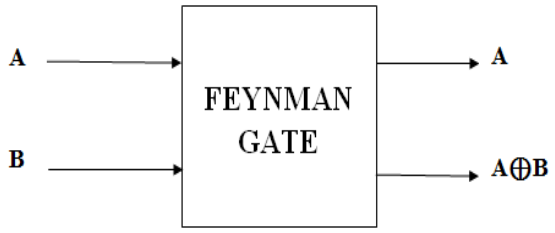



Figure 3.1 Feynman Gate

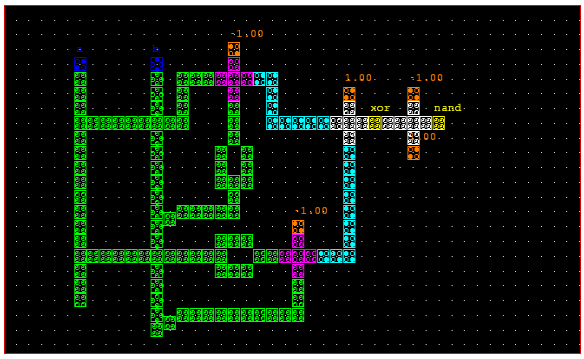


Figure 3.2 Feynman gate circuit

### B. Design a reversible decoder in QCA

Feynman Gate based 4 to 16 decoder can be designed in QCA.In this Reversible decoder area can be minimized and it offers a higher speed [7].

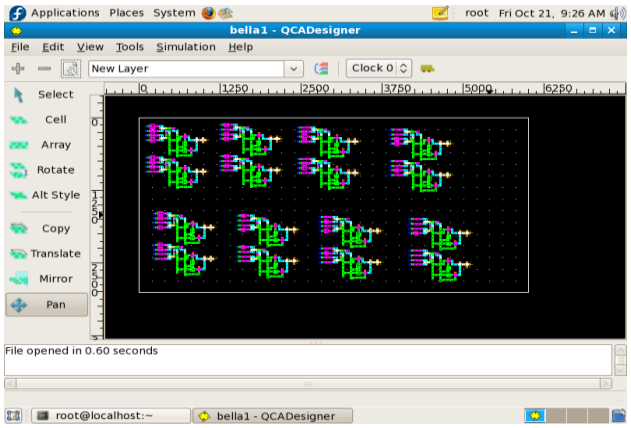
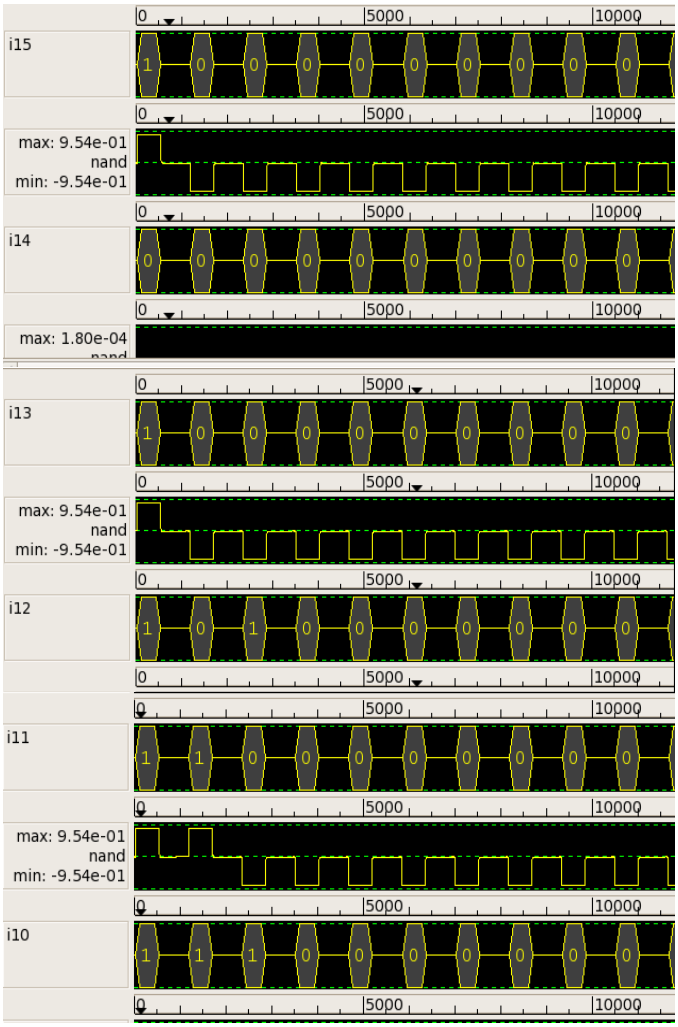



Figure 3.3 Reversible Decoder

## 4. SIMULATION RESULTS

The output of Feynman Gate based reversible decoder shown in fig.4.Total simulation time for reversible decoder is 30s.



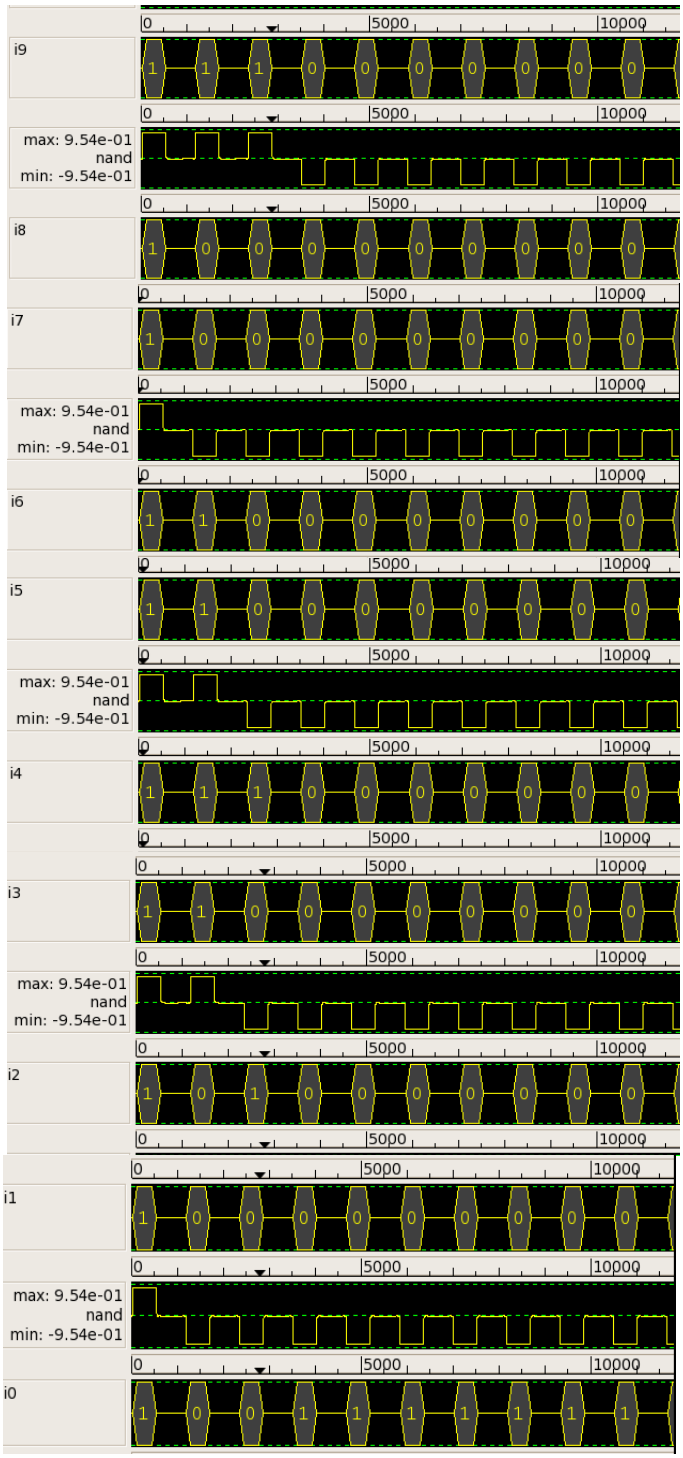



Figure 4 Simulation results

## 5. COMPARISON RESULTS

The simulation results regarding Cell Count, Area are listed in Table I, Table and II. In reversible Decoder Area can be minimized.

TABLE-I
COMPARISION OF REVERSIBLE GATES COMPLEXITY

| S.NO | Reversible Gate | No of cells(complexity) | Area(μm) |
|---|---|---|---|
| 1 | Toffoli gate | 183 | 0.39 |
| 2 | Feynman gate | 143 | 0.26 |

TABLE-II
COMPARISON OF AREA

| S.NO | Decoder | Cell count | Area(μm) |
|---|---|---|---|
| 1 | 2 to 4 decoder | 808 | 2.32 |
| 2 | 4 to 16 decoder | 3968 | 13.79 |

## 6. CONCLUSION

The design under consideration, i,e reversible decoder is said to be an area effective when designed with QCA rather than CMOS. As there is an advantage of both low area and power at the same abstraction level, QCA can be seen as one of the promising technologies in near future. However there is still research going on in the inter disciplines of physical implementations and cost effective manufacturing process. High speed decoder is the essential components in fast SRAM[9].The work can be extended to design a SRAM which will be highly delay efficient design.

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